Amdt. Dated January 2, 2004

Reply to Office Action of September 2, 2003

CLAIM AMENDMENTS

Claim 1 (currently amended): A method of synchronizing mobile CDMA radio receivers in a cellular CDMA mobile radio system, wherein a first synchronization channel with a first frequency is provided for transmitting a synchronization signal with a code that is known to the mobile radio receivers and to base stations of the mobile radio system, and wherein a transmission from a base station to a mobile radio receiver delays the synchronization signal by an unknown time period and the first frequency is shifted by the transmission to a second frequency, the method which comprises the following steps:

splitting the received synchronization signal into a real part signal and an imaginary part signal;

sampling the real part signal and the imaginary part signal to form sampled signals;

digitally filtering each sampled signal to correlate the sampled signal to the known code and to form filtered signals;

squaring each filtered signal to form squared signals;

determining a maximum signal level from the squared signals;



Amdt. Dated January 2, 2004

Reply to Office Action of September 2, 2003

estimating the unknown time period with the maximum signal level determined in the determining step;

despreading the received synchronization signal with the known code and taking into account the time period estimated in the estimating step;

determining a frequency deviation between the first frequency and the second frequency based on the despread received synchronization signal; and

fine-tuning the second frequency to the first frequency <u>based</u>
in part on the despread received synchronization signal.

Claim 2 (original): The method according to claim 1, wherein the filtering step comprises delaying the sampled values of each signal by up to (2K+1) clock cycles, where K is a number of coefficients of a digital filter executing the filtering step.

Claim 3 (original): The method according to claim 2, which comprises multiplying the differently delayed sampled values by 2(K+1) coefficients and then summing.

Amdt. Dated January 2, 2004

Reply to Office Action of September 2, 2003

Claim 4 (original): The method according to claim 3, wherein the 2(K+1) coefficients have (K+1) pairs of identical coefficients.

Blok.

Claim 5 (previously presented): The method according to claim 1, which comprises defining the code to be transmitted with the synchronization signal to have a sequence of 256 chips uniquely characterizing the first synchronization channel.

Claim 6 (original): The method according to claim 5, which comprises sampling each signal obtained by splitting with a sampling rate wherein two sampled values are taken per chip of the code.

Claim 7 (previously presented). A device for synchronizing mobile CDMA radio receivers using the method according to claim 1 in a mobile radio system having a first synchronization channel for transmitting a synchronization signal with a code that is known to all the mobile radio

Amdt. Dated January 2, 2004

Reply to Office Action of September 2, 2003

receivers and to all base stations of the mobile radio system, comprising:

input signal processing units in a mobile radio receiver for processing the received synchronization signal including a real part signal and an imaginary part signal;

said input signal processing units generating sampled values;

Blook

a plurality of delay circuits connected in series with said input signal processing units for receiving an input signal and outputting an output signal, said delay circuits receiving the sampled values and correlating the real part signal and the imaginary part signal with the known code;

multipliers connected to receive the input signal and the output signal of each delay circuit and multiplying a supplied signal with a coefficient;

a first adder connected to receive an output signal from each said multiplier, said first adder outputting a summed signal;

squaring elements each having an input connected to receive the summed signal from a respective said first adder and outputting a squared signal; and

a second adder connected to receive the squared signals from said squaring elements.

Amdt. Dated January 2, 2004

Reply to Office Action of September 2, 2003

Claim 8 (original): The device according to claim 7, wherein each said input signal processing unit has an analog low-pass filter, a sampler, and a memory.

Claim 9 (original): The device according to claim 7, wherein a number of different coefficients is (K+1).

Blook

Claim 10 (original): The device according to claim 9, wherein 2(K+1) multipliers are provided, and two multipliers in each case multiply signals received thereby by one of the (K+1) different coefficients.

Claim 11 (original): The device according to claim 10, wherein in each case two multipliers are connected to multiply one of the input signal and the output signal of one of said delay circuits by one of the (K+1) different coefficients.

Claim 12 (previously presented): The method according to claim 1, wherein the first synchronization channel is a

Amdt. Dated January 2, 2004 Reply to Office Action of September 2, 2003

primary synchronization channel PSCH stipulated in a UMTS

standard.